EAST SEARCH

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L#	Hits	Search String	Databases
L1	1593	dynamic and (power adj dissipation) and ((integrated adj circuit) or ic) and (simulat$6 or model$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	100	1 and (dynamic near10 (power adj dissipation))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	22	2 and (annotat$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Results of search set L2:

US RE31545 E	Feed-forward amplifier	19840327	330/149
US 6735683 B2	Single-chip microcomputer with hierarchical internal bus structure having data and address signal lines coupling CPU with other processing elements	20040511	712/1
US 6728941 B2	Method of modeling the crossover current component in submicron CMOS integrated circuits designs	20040427	716/5
US 6717461 B2	Circuits with dynamic biasing	20040406	327/552
US 6683492 B2	Circuits with dynamic biasing	20040127	327/552
US 6642543 B1	Thin and thick gate oxide transistors on a functional block of a CMOS circuit residing within the core of an IC chip	20031104	257/72
US 6605806 B2	System and method for generating signals representing infrared radiation	20030812	250/332
US 6592764 B1	Block copolymer processing for mesostructured inorganic oxide materials	20030715	210/660
US 6591294 B2	Processing system with microcomputers each operable in master and slave modes using configurable bus access control terminals and bus use priority signals	20030708	709/209
US 6578176 B1	Method and system for genetic algorithm based power optimization for integrated circuit designs	20030610	716/2
US 6559681 B1	Resonant logic and the implementation of low power digital integrated circuits	20030506	326/98
US 6542846 B1	Thermal management system for a portable ultrasound imaging device	20030401	702/132
US 6529861 B1	Power consumption reduction for domino circuits	20030304	703/14
US 6513137 B1	Test method and apparatus using energy consumption ratio	20030128	714/736
US 6493863 B1	Method of designing semiconductor integrated circuit	20021210	716/18
US 6448816 B1	Resonant logic and the implementation of low power digital integrated circuits	20020910	326/98
US 6417705 B1	Output driver with DLL control of output driver strength	20020709	327/158
US 6415181 B1	Implantable medical device incorporating adiabatic clock-powered logic	20020702	607/16
US 6397170 B1	Simulation based power optimization	20020528	703/14
US 6396137 B1	Integrated voltage/current/power regulator/switch system and method	20020528	257/691
US 6389507 B1	Memory device search system and method	20020514	711/108

US 6373340 B1	High-efficiency audio power amplifier	20020416	330/297
US 6366061 B1	Multiple power supply circuit architecture	20020402	323/223
US 6346427 B1	Parameter adjustment in a MOS integrated circuit	20020212	438/10
US 6345379 B1	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	20020205	716/4
US 6333656 B1	Flip-flops	20011225	327/202
US 6324678 B1	Method and system for creating and validating low level description of electronic design	20011127	716/18
US 6304130 B1	Bias circuit for depletion mode field-effect transistors	20011016	327/430
US 6297668 B1	Serial device compaction for improving integrated circuit layouts	20011002	326/101
US 6285247 B1	Optimized low voltage CMOS operation	20010904	327/544
US 6252448 B1	Coincident complementary clock generator for logic circuits	20010626	327/259
US 6216252 B1	Method and system for creating, validating, and scaling structural description of electronic device	20010410	716/1
US 6212665 B1	Efficient power analysis method for logic cells with many output switchings	20010403	716/4
US 6198324 B1	Flip flops	20010306	327/202
US 6181123 B1	Digital programmable direct current to direct current (DC-DC) voltage-down converter	20010130	323/351
US 6163174 A	Digital buffer circuits	20001219	326/108
US 6157903 A	Method of minimizing macrocell characterization time for state dependent power analysis	20001205	703/14
US 6100716 A	Voltage excursion detection apparatus	20000808	326/68
US 6087886 A	Hybrid dual threshold transistor multiplexer	20000711	327/408
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US 5982211 A	Hybrid dual threshold transistor registers	19991109	327/202
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US 5818261 A	Pseudo differential bus driver/receiver for field programmable devices	19981006	326/86
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US 5740407 A	Method of generating power vectors for circuit power dissipation simulation having both combinational and sequential logic circuits	19980414	703/13

US 5701094 A	Logic circuits for wave pipelining	19971223	326/113
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US 4146844 A	Feed-forward amplifier	19790327	330/149
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US 20030217297 A1	Method and apparatus for software-assisted thermal management for electronic systems	20031120	713/300
US 20030210101 A1	MEMS-based, computer systems, clock generation and oscillator circuits and LC-tank apparatus for use therein	20031113	331/117FE
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100 **An oldest-first selection logic implementation for non-compacting issue queues [microprocessor power reduction]**
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Terms used **dynamic** and **power dissipation** and **integrated circuit** or **ic** and **simulat** or **model**

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1 Power minimization in IC design: principles and applications
Massoud Pedram
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1
Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

2 System-level power optimization: techniques and tools
Luca Benini, Giovanni de Micheli
April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2
Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

3 IC test using the energy consumption ratio
Wanli Jiang, Bapiraju Vinnakota
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation conference**
Full text available: pdf(89.67 KB) Additional Information: full citation, references, citings, index terms

4 Keynote speech 1: Elements of low power design for integrated systems
Sung-Mo Kang

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(281.58 KB) Additional Information: full citation, abstract, references, index terms

The increasing prominence of portable systems and the need to limit power consumption and hence, heat dissipation in very high density VLSI chips have led to rapid and innovative developments in low power design recently. Leakage control is becoming critically important for deep sub-100nm technologies due to the scaling down of threshold voltage and gate oxide thickness of transistors. In this paper, we discuss major sources of power dissipation in VLSI systems, and various low power design tech ...

Keywords: CMOS, VLSI, low power integrated circuits

5 Power estimation techniques for integrated circuits

Farid N. Najm

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(218.32 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

With the advent of portable and high-density microelectronic devices, the power dissipation of very large scale integrated (VLSI) circuits is becoming a critical concern. Accurate and efficient power estimation during the design phase is required in order to meet the power specifications without a costly redesign process. Recently, a variety of power estimation techniques have been proposed, most of which are based on: 1) the use of simplified delay models, and 2) modeling the long-term behavior ...

Keywords: power estimation VLSI circuit survey tutorial probability statistics

6 Interconnect analysis for SoCs and microprocessors: Interconnect-power dissipation in a microprocessor

Nir Magen, Avinoam Kolodny, Uri Weiser, Nachum Shamir

February 2004 **Proceedings of the 2004 international workshop on System level interconnect prediction**

Full text available: pdf(249.61 KB) Additional Information: full citation, abstract, references, index terms

Interconnect power is dynamic power dissipation due to switching of interconnection capacitances. This paper describes the characterization of interconnect power in a state-of-the-art high-performance microprocessor designed for power efficiency. The analysis showed that interconnect power is over 50% of the dynamic power. Over 90% of the interconnect power is consumed by only 10% of the interconnections. Relations of interconnect power to wire length distribution and hierarchy level of nets wer ...

Keywords: Interconnect power, low-power design, routing, wire spacing

7 Session 10C: Embedded tutorial: IC power distribution challenges: IC power distribution challenges

Sudhakar Bobba, Tyler Thorp, Kathirgamar Aingaran, Dean Liu

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(125.96 KB) Additional Information: full citation, abstract, references, citings, index terms

With each technology generation, delivering a timevarying current with reduced nominal supply voltage variation is becoming more difficult due to increasing current and power requirements. The power delivery network design becomes much more complex and requires accurate analysis and optimizations at all levels of abstraction in order to meet the specifications. In this paper, we describe techniques for estimation of the supply voltage variations that can be used in the design of the power delive ...

8 Challenges in integrated CMOS transceivers for short distance wireless

Khurram Muhammad, Robert B. Straszewski, Poras T. Balsara

March 2001 **Proceedings of the 11th Great Lakes Symposium on VLSI**

Full text available: pdf(797.97 KB) Additional Information: full citation, references, index terms

9 Low power RF integrated circuits: principles and practice
A. A. Abidi, H. Darabi
August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**
Full text available: pdf(191.14 KB) Additional Information: full citation, references, index terms

10 Iterative schedule optimization for voltage scalable distributed embedded systems
Marcus T. Schmitz, Bashir M. Al-Hashimi, Petru Eles
February 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 1
Full text available: pdf(273.28 KB) Additional Information: full citation, abstract, references, index terms

We present an iterative schedule optimization for multirate system specifications, mapped onto heterogeneous distributed architectures containing dynamic voltage scalable processing elements (DVS-PEs). To achieve a high degree of energy reduction, we formulate a generalized DVS problem, taking into account the power variations among the executing tasks. An efficient heuristic is presented that identifies optimized supply voltages by not only "simply" exploiting slack time, but under the addition ...

Keywords: Dynamic voltage scaling, embedded systems, energy minimization, heterogeneous distributed systems, scheduling, system synthesis

11 Architecture Analysis and Automation: Dynamic power consumption in Virtex™-II FPGA family
Li Shang, Alireza S. Kaviani, Kusuma Bathala
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Full text available: pdf(309.07 KB) Additional Information: full citation, abstract, references, citings

This paper analyzes the dynamic power consumption in the fabric of Field Programmable Gate Arrays (FPGAs) by taking advantage of both simulation and measurement. Our target device is Xilinx Virtex™-II family, which contains the most recent and largest programmable fabric. We identify important resources in the FPGA architecture and obtain their utilization, using a large set of real designs. Then, using a number of representative case studies we calculate the switching activity correspondi ...

12 Mixed-signal design and simulation: A 16-bit mixed-signal microsystem with integrated CMOS-MEMS clock reference
Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Gebara, Keith L. Kraver, Matthew R. Guthaus, Richard B. Brown
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(793.60 KB) Additional Information: full citation, abstract, references, index terms

In this work, we report on an unprecedented design where digital, analog, and MEMS technologies are combined to realize a general-purpose single-chip CMOS microsystem. The convergence of these technologies has enabled the development of a low power, portable microinstrument ideally suited for controlling environmental and bio-implantable sensors.

Keywords: ADC, MEMS, PGA, SD, SoC, clock generation, design methodology, inductor, low power, low voltage analog, microcontroller, microsystem, mixed-signal, system-on-chip, varactor

13 Getting to the bottom of deep submicron
Dennis Sylvester, Kurt Keutzer
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(1.22 MB) Additional Information: full citation, references, citings, index terms

Keywords: ASIC, CMOS scaling, gate delay, interconnect modeling, power dissipation, signal integrity, wirelength

14 Future performance challenges in nanometer design
Dennis Sylvester, Himanshu Kaul
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(252.60 KB) Additional Information: full citation, abstract, references, citings, index terms

We highlight several fundamental challenges to designing high-performance integrated circuits in nanometer-scale technologies (i.e. draRita Glover, EDA Today, L.C.wn feature sizes< 100 nm). Dynamic power scaling trends lead to major packaging problems. To alleviate these concerns, tMarc Halpernhermal monitoring and feedback mechanisms can limit worst-case dissipation and reduce costs. Furthermore, a flexible multi-Vdd + multi-Vth + re-sizing approach is advocated to leverage the inherent pr ...

15 Leakage Current: Leakage current in low standby power and high performance devices: trends and challenges
Geoffrey C-F Yeap
April 2002 **Proceedings of the 2002 international symposium on Physical design**

Full text available: pdf(212.42 KB) Additional Information: full citation, abstract, references, index terms

IC technology is continuing to scale according to Moore's Law, with the overall chip circuit requirements driving the MOSFET device and process integration requirements and optimal choices. In the 2001 International Technology Roadmap for Semiconductors (ITRS) [1] the driver for the high performance logic is maximizing MOSFET intrinsic speed, while the driver for low standby power logic is minimizing MOSFET leakage current. Total leakage current of a MOSFET consists of three components: off-stat ...

Keywords: CMOS technology, gate tunneling leakage, high performance, leakage current, low standby power, off-state sub-threshold leakage, system-on-a-ship (SoC)

16 Technology decomposition and mapping targeting low power dissipation
Chi-Ying Tsui, Massoud Pedram, Alvin M. Despain
July 1993 **Proceedings of the 30th international on Design automation conference**

Full text available: pdf(657.86 KB) Additional Information: full citation, references, citings, index terms

17 Keynote speech 4: Low power RF IC design for wireless communication
Domine M.W. Leenaerts
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, index terms

In this paper, the many issues around the system and circuit design of advanced RF front ends for wireless RF applications will be discussed. After a short discussion on technology related issues, design choices linked to the different circuit/system solutions will be discussed.

Keywords: LNA, PLL, RF, VCO, low power, technology, transceivers, wireless communication

18 Wireless telecom silicon integration: analog design for radio, baseband and speech spectrum
J. Sevenhans, D. Haspeslagh, J. Wenin
January 1998 **Wireless Networks**, Volume 4 Issue 1

Full text available: pdf(324.74 KB) Additional Information: full citation, abstract, references, index terms

The application today, pushing analog design for CMOS and RF-bipolar into new frontiers is definitely the mobile radio telephony. New telecom systems like GSM, PCN, DECT, DCS, Wireless in the loop...are all developing very rapidly and will enable us very soon to organise a complete telephone network with full coverage for your car, as well as in your kitchen and on your office desk. In Europe the major telecom companies have worked together to establish one common standard for cellular mobi ...

19 What is the state of the art in commercial EDA tools for low power?
K. Keutzer, O. Coudert, R. Haddad
August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**
Full text available: pdf(196.98 KB) Additional Information: full citation, references, citings, index terms

20 Tools and architectures for power minimization: Active leakage power optimization for FPGAs
Jason H. Anderson, Farid N. Najm, Tim Tuan
February 2004 **Proceeding of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**
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We consider active leakage power dissipation in FPGAs and present a "no cost" approach for active leakage reduction. It is well-known that the leakage power consumed by a digital CMOS circuit depends strongly on the state of its inputs. Our leakage reduction technique leverages a fundamental property of basic FPGA logic elements (look-up-tables) that allows a logic signal in an FPGA design to be interchanged with its complemented form without any area or delay penalty. We apply this property to ...

Keywords: FPGAs, field-programmable gate arrays, leakage, low-power design, optimization, power

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